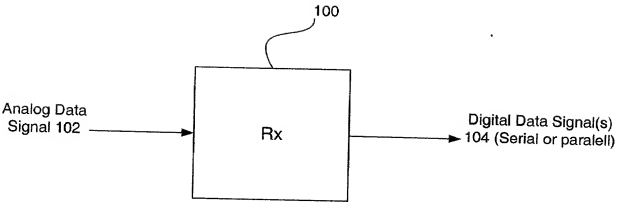

100
Analog Data
Signal 102
Rx
Digital Data Signal(s)
104 (Serial or paralell)

FIG. 1

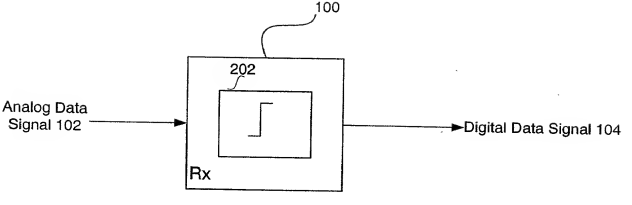
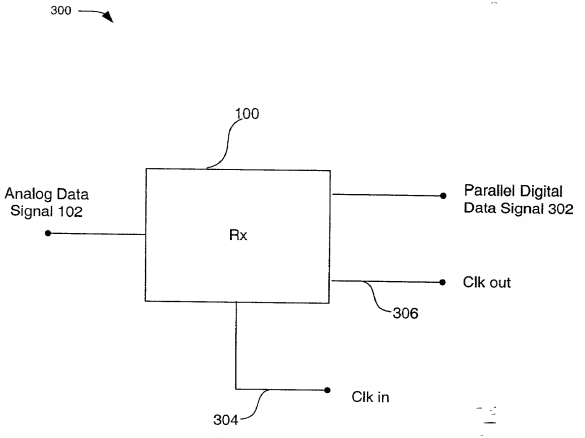


FIG. 2



Serial-to-Parallel Receiver

FIG. 3

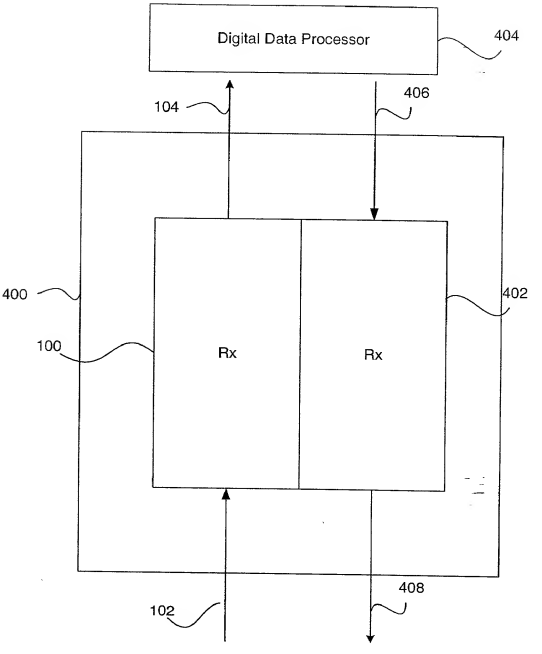


FIG. 4

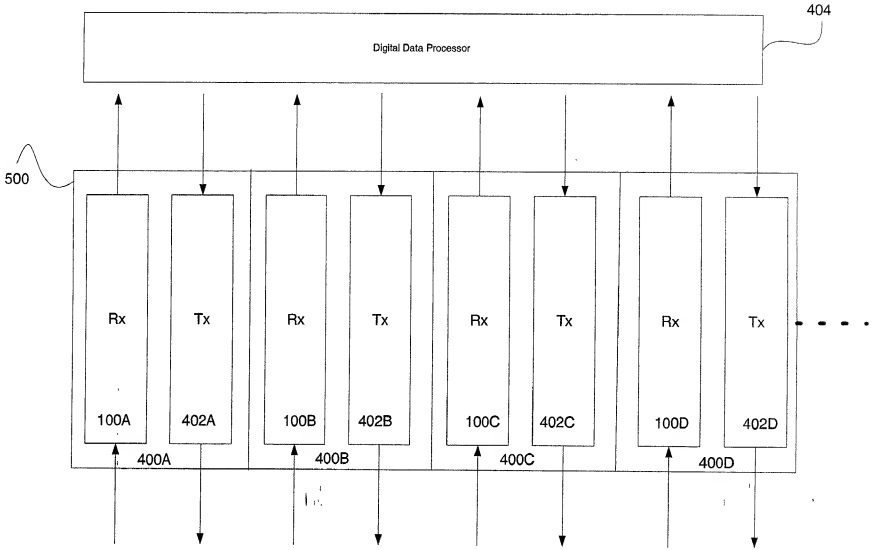

404
Digital Data Processor
500
Rx
Tx
Rx
Tx
Rx
Tx
Rx
Tx
100A
402A
100B
402B
100C
402C
100D
402D
400A
400B
400C
400D

FIG. 5

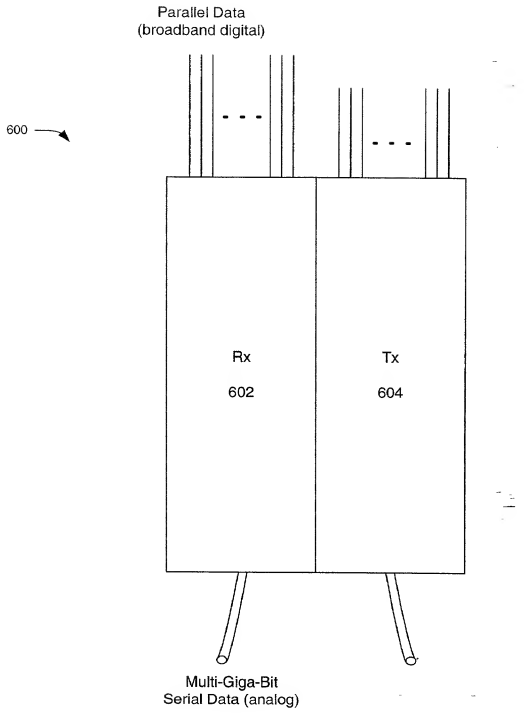

Parallel Data
(broadband digital)
600
Rx
602
Tx
604
Multi-Giga-Bit
Serial Data (analog)

FIG. 6

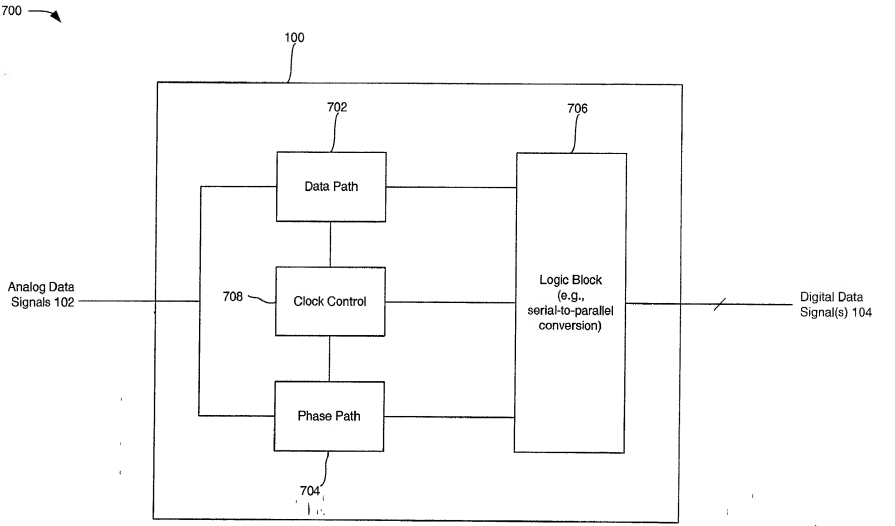


FIG. 7

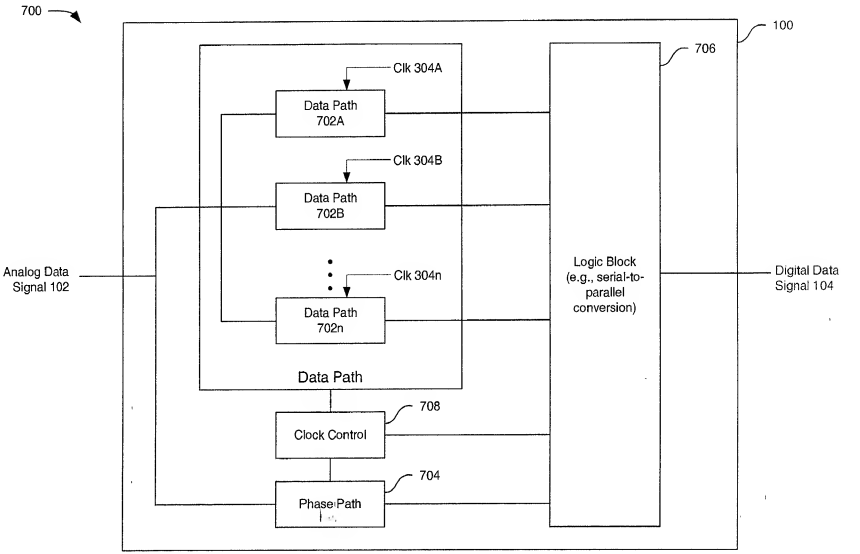


FIG. 8

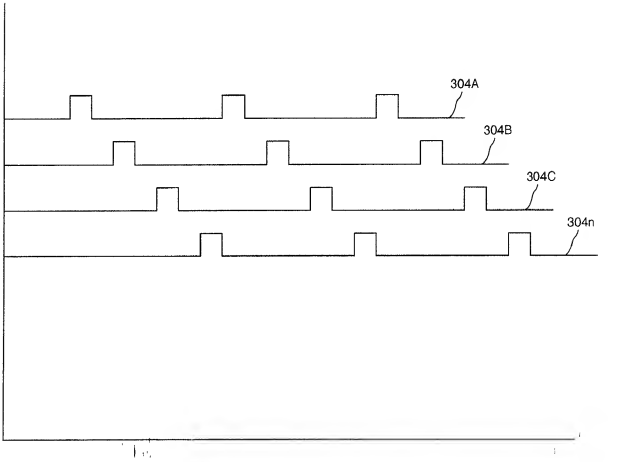


FIG. 9

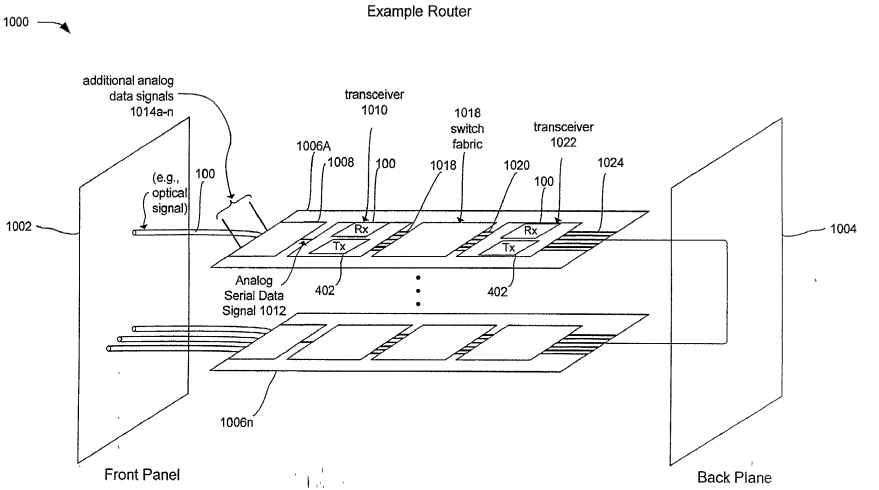


FIG. 10

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
No Equalization

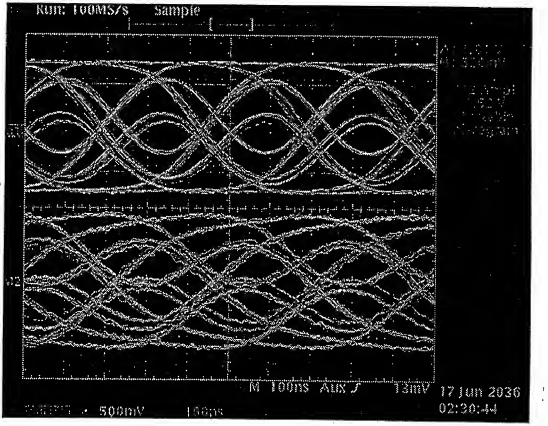


FIG. 11A

Firewire
25-feet IEEE 1394
No Equalization

FIG. 11B

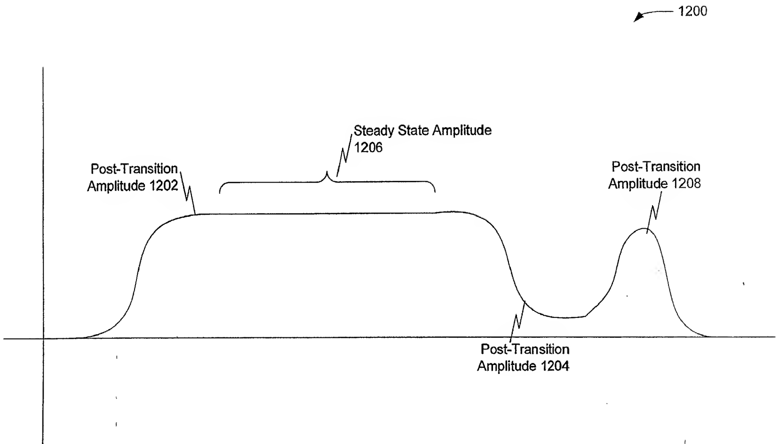

1200
Steady State Amplitude 1206
Post-Transition Amplitude 1202
Post-Transition Amplitude 1208
Post-Transition Amplitude 1204

FIG. 12

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
Equalization
a = 0.25
Eye Opening = 900mV

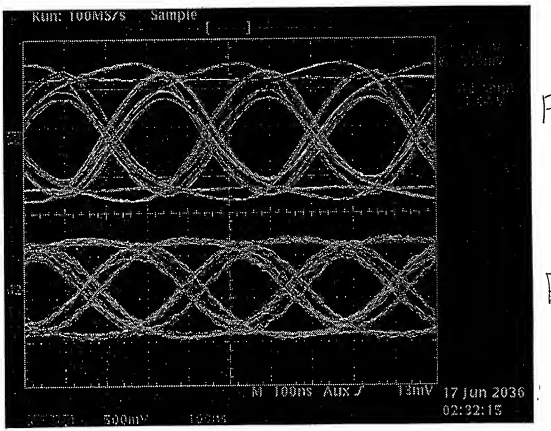


FIG 13A

Firewire
25-feet IEEE 1394
Equalization
a = 0.375
Eye Opening = 750mV

FIG. 13B

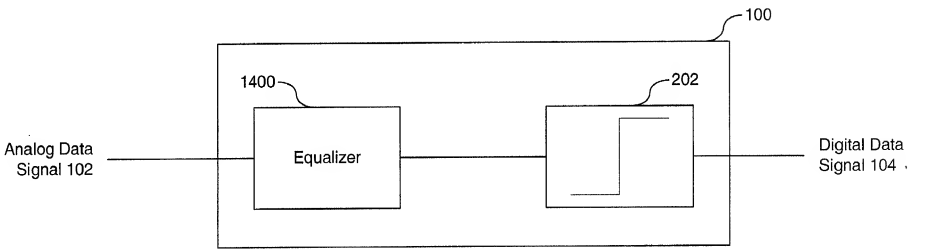

100
1400
202
Equalizer
Analog Data
Signal 102
Digital Data
Signal 104

FIG. 14

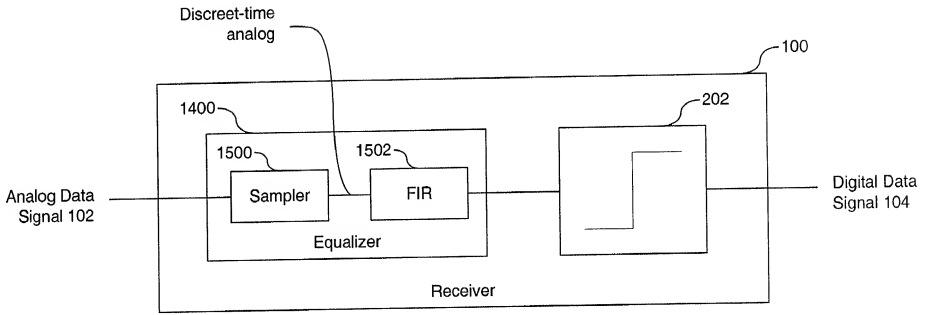


FIG. 15

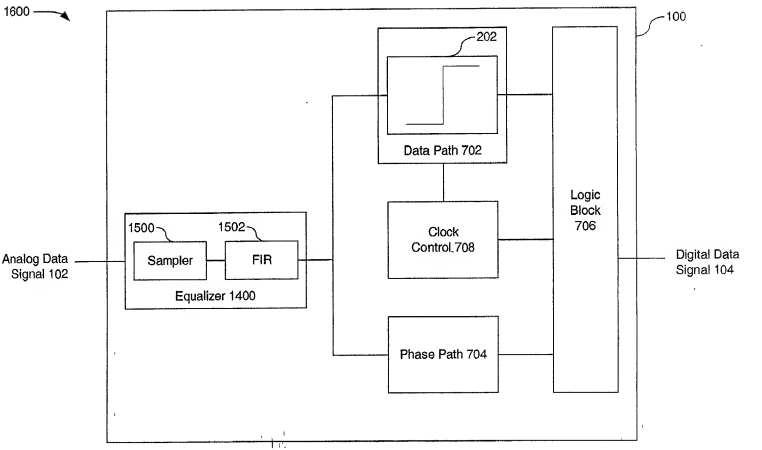


FIG. 16

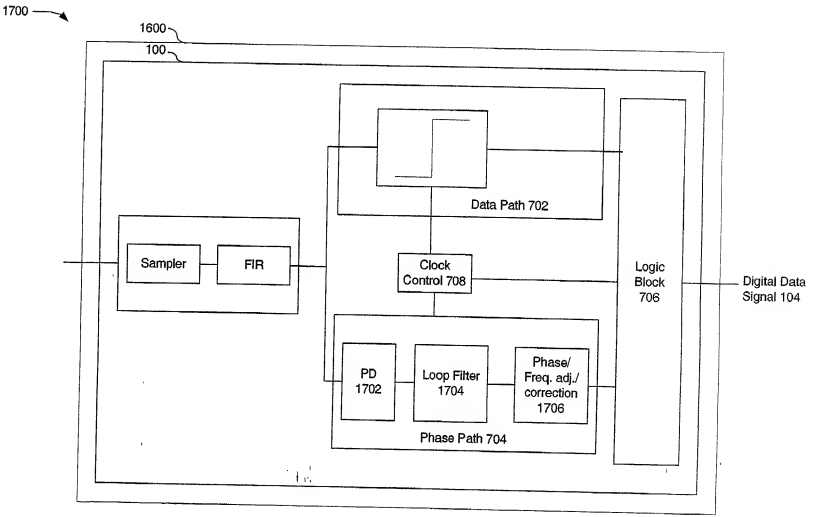


FIG. 17

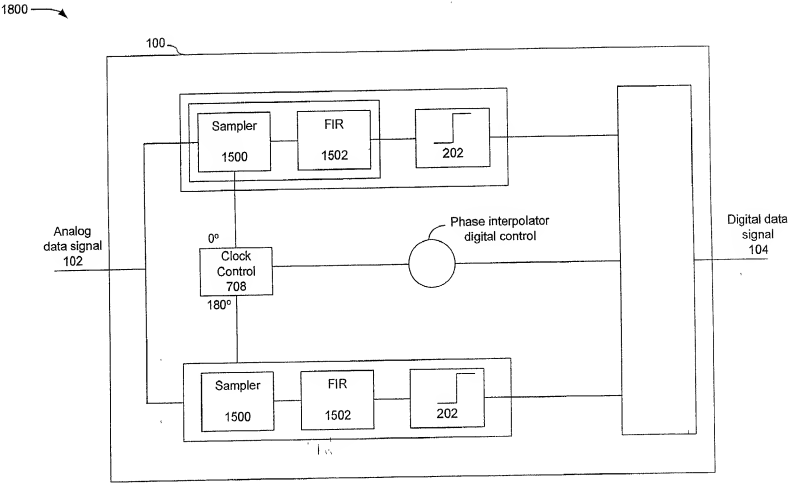


FIG. 18

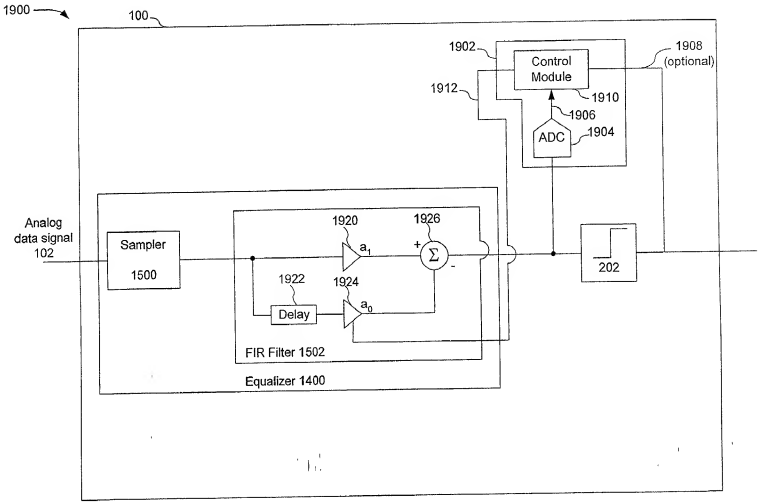


FIG. 19

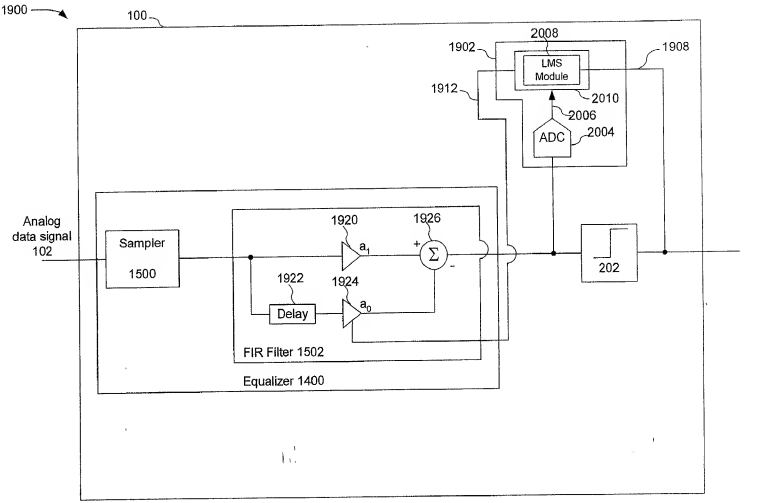


FIG. 20

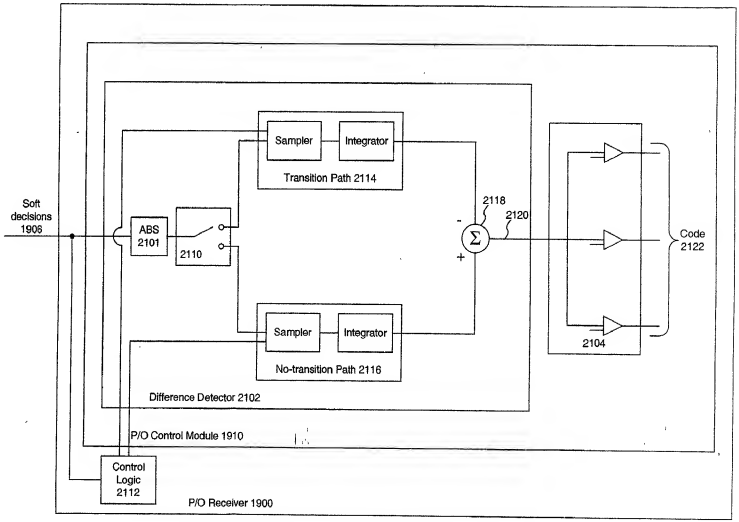


FIG. 21A

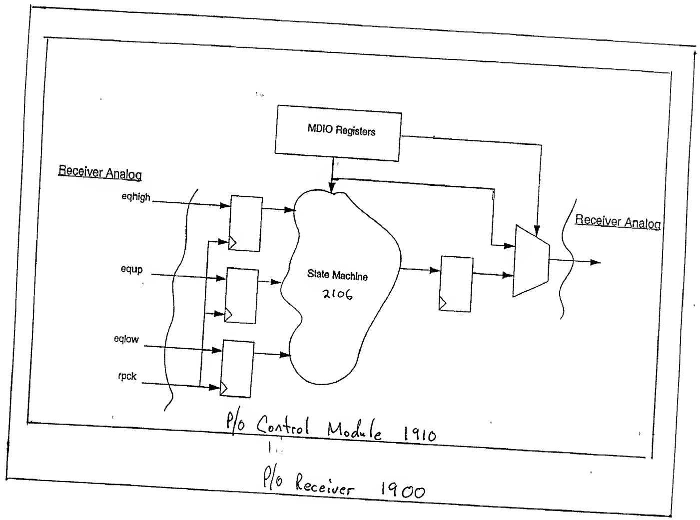

MDIO Registers
Receiver Analog
eqhigh
equp
eqlow
rpck
State Machine
2106
Receiver Analog
P/O Control Module 1910
P/O Receiver 1900

FIG. 21 B

Adaptive equalizer control logic

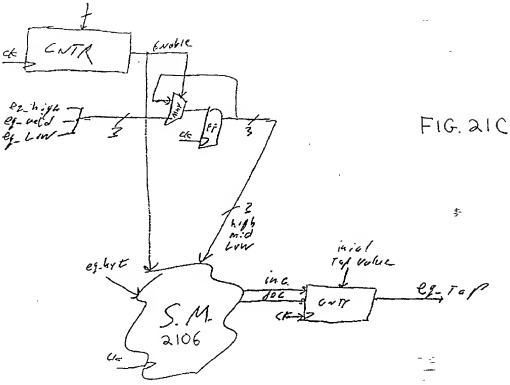


FIG. 21C

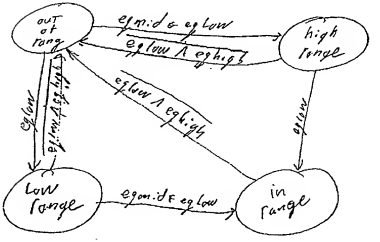


FIG. 21D

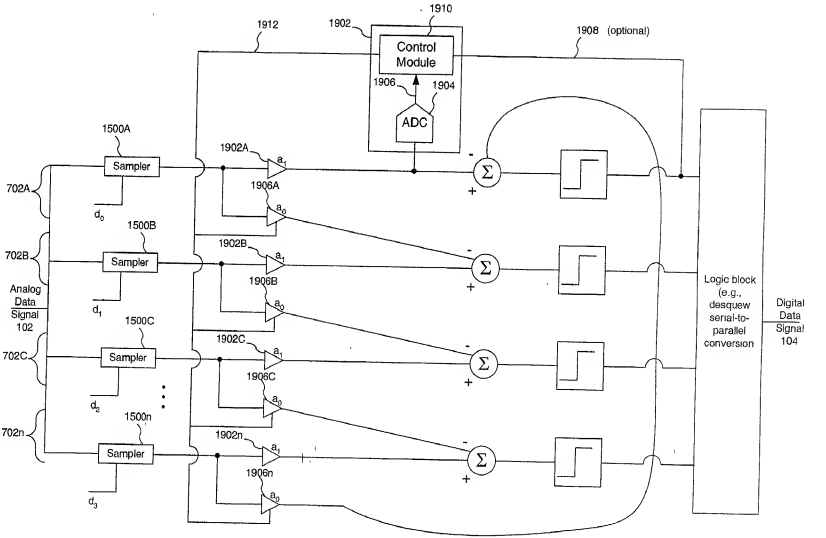


FIG. 22

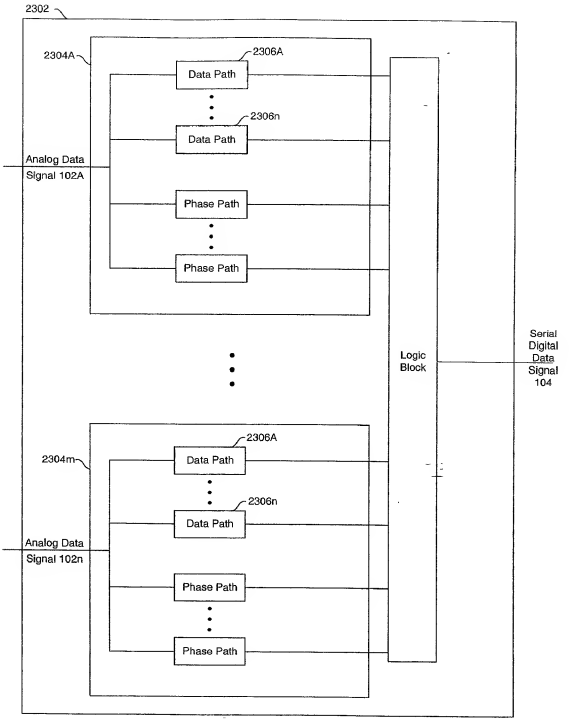

2302
2304A
2306A
Data Path
2306n
Data Path
Analog Data Signal 102A
Phase Path
Phase Path
Logic Block
Serial Digital Data Signal 104
2304m
2306A
Data Path
2306n
Data Path
Analog Data Signal 102n
Phase Path
Phase Path

FIG. 23

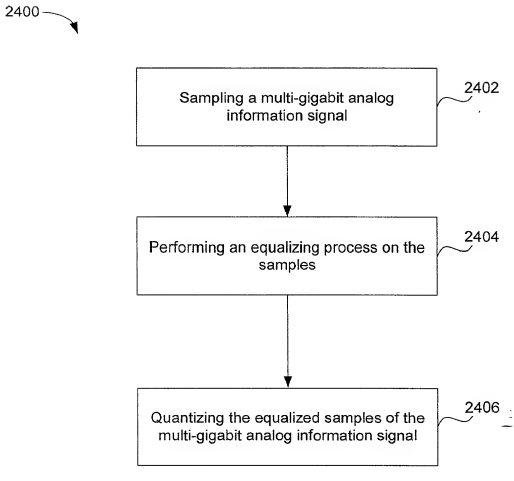

2400
Sampling a multi-gigabit analog information signal
2402
Performing an equalizing process on the samples
2404
Quantizing the equalized samples of the multi-gigabit analog information signal
2406

FIG. 24

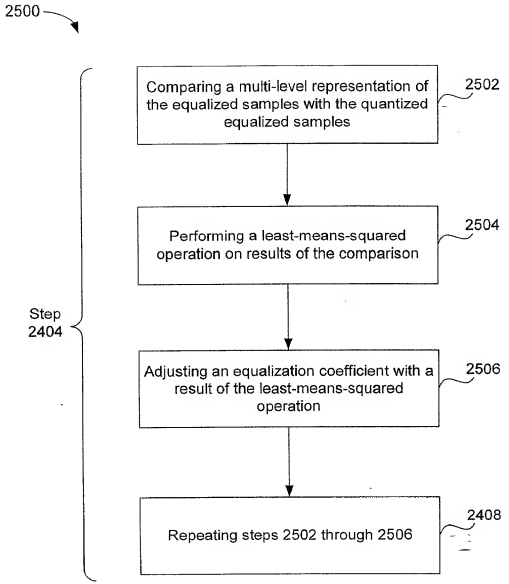

2500
Comparing a multi-level representation of the equalized samples with the quantized equalized samples
2502
Performing a least-means-squared operation on results of the comparison
2504
Step 2404
Adjusting an equalization coefficient with a result of the least-means-squared operation
2506
Repeating steps 2502 through 2506
2408

FIG. 25

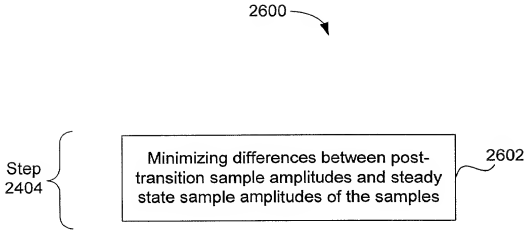

2600
Step
2404
Minimizing differences between post-transition sample amplitudes and steady state sample amplitudes of the samples
2602

FIG. 26

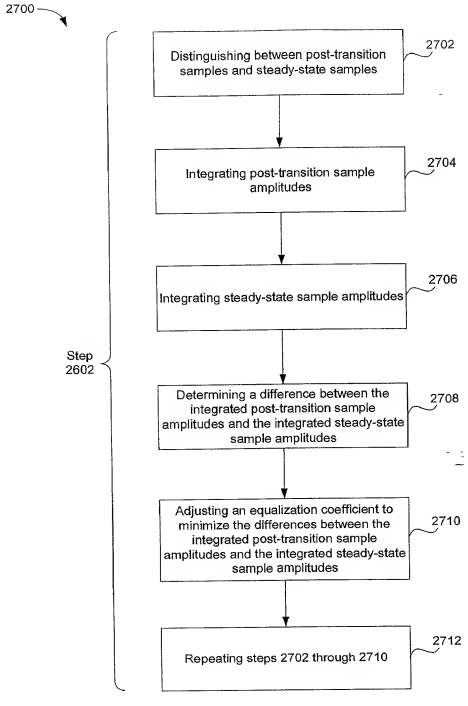

2700
Distinguishing between post-transition samples and steady-state samples
2702
Integrating post-transition sample amplitudes
2704
Integrating steady-state sample amplitudes
2706
Step 2602
Determining a difference between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2708
Adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2710
Repeating steps 2702 through 2710
2712

FIG. 27

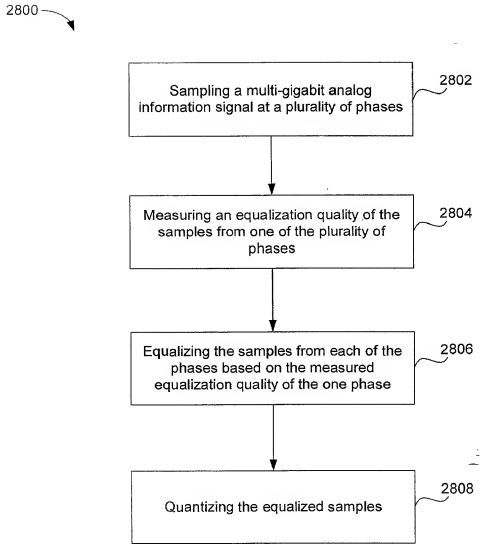

2800
Sampling a multi-gigabit analog information signal at a plurality of phases
2802
Measuring an equalization quality of the samples from one of the plurality of phases
2804
Equalizing the samples from each of the phases based on the measured equalization quality of the one phase
2806
Quantizing the equalized samples
2808

FIG. 28

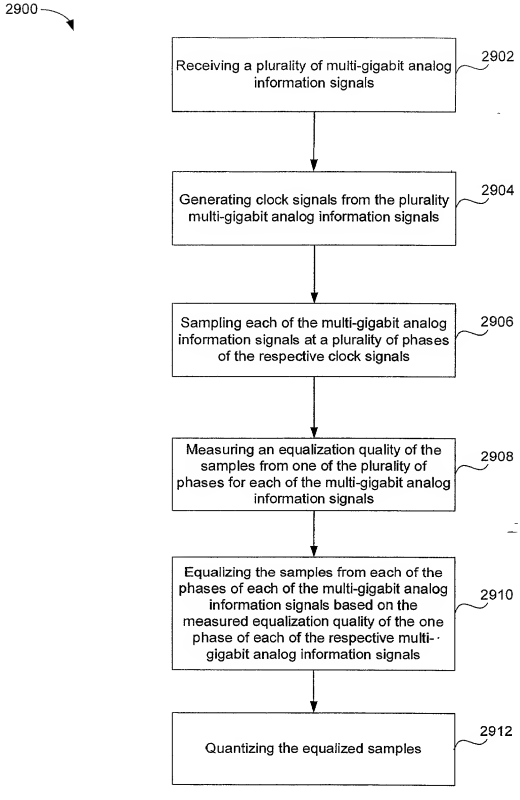

2900
Receiving a plurality of multi-gigabit analog information signals
2902
Generating clock signals from the plurality multi-gigabit analog information signals
2904
Sampling each of the multi-gigabit analog information signals at a plurality of phases of the respective clock signals
2906
Measuring an equalization quality of the samples from one of the plurality of phases for each of the multi-gigabit analog information signals
2908
Equalizing the samples from each of the phases of each of the multi-gigabit analog information signals based on the measured equalization quality of the one phase of each of the respective multi-gigabit analog information signals
2910
Quantizing the equalized samples
2912

FIG. 29

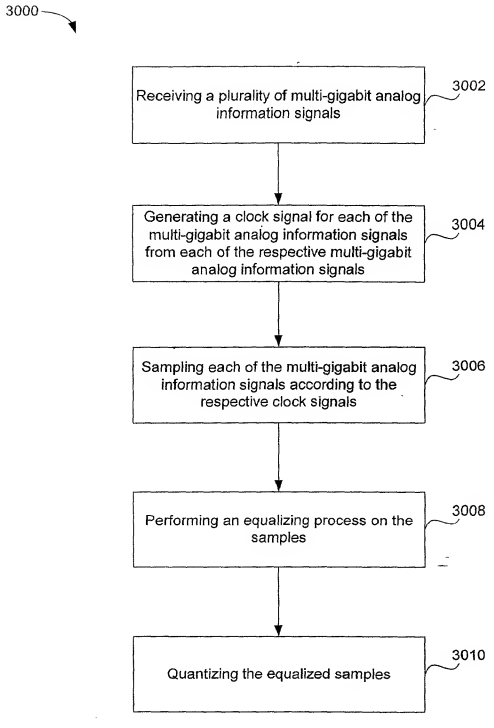

3000
Receiving a plurality of multi-gigabit analog information signals
3002
Generating a clock signal for each of the multi-gigabit analog information signals from each of the respective multi-gigabit analog information signals
3004
Sampling each of the multi-gigabit analog information signals according to the respective clock signals
3006
Performing an equalizing process on the samples
3008
Quantizing the equalized samples
3010

FIG. 30